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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/008,653	11/09/2001	Fernando Gonzalez	98095DIV4	8023

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KIRKPATRICK & LOCKHART NICHOLSON GRAHAM LLP
535 SMITHFIELD STREET
PITTSBURGH, PA 15222

EXAMINER	
RICHARDS, N DREW	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 02/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/008,653	GONZALEZ ET AL.	
	Examiner	Art Unit	
	N. Drew Richards	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *17,98-103,125,126 and 128* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *17,98-103,125,126 and 128* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 17, 98-101, 103, 125, 126 and 128 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moravvej-Farshi et al. ("Novel Self-Aligned Polysilicon-Gate MOSFETs with Polysilicon Source and Drain," Solid-State Electronics, Vol. 30, No. 10, 1987, Pp. 1053-62) in view of Wolf et al. ("Silicon Processing for the VLSI Era, Volume 3: The Submicron MOSFET," 1995, Pp. 232-240 and 309-311).

Moravvej-Farshi et al. disclose in figure 6 a raised drain structure (n+ poly), a raised source structure (n+ poly), a gate (n+ poly) located between the source and drain, a first capping layer (silicon dioxide on left half of figure) in communication with at least a portion of the gate and source, a first portion of a gate oxide region in communication with at least a portion of the gate and source, a second capping layer (silicon dioxide on right half of figure) in communication with at least a portion of the gate and drain, and a second portion of a gate oxide region in communication with at least a portion of the gate and drain. Moravvej-Farshi et al. do not teach a first pocket implant junction located in the substrate assembly comprising a first high dose implant and defining a first low-resistance path wherein the first pocket implant junction is in communication with a non-sidewall portion of the source and extends under a first

portion of the gate. Nor does Moravvej-Farshi et al. teach a second pocket implant junction located in the substrate assembly comprising a second high dose implant and defining a second low-resistance path wherein the second pocket implant junction is in communication with a non-sidewall portion of the drain and extends under a first portion of the gate.

Wolf et al. teach a transistor formed on a substrate assembly in figure 5-25(c), for example. Wolf et al. teach a source, drain, polysilicon gate between the source and drain, a gate oxide, and first and second pocket implant junctions. As seen in figure 5-25(c) P-type pocket implant junctions are formed in the substrate assembly by first and second high dose implants, thus defining a low-resistance path, and the pocket implant junctions are in communication with a non-sidewall portion of the source and drain and extend under a portion of the gate. As seen in figure 5-25(c), the p+ pocket implants extend a short distance under the source and drain, this short distance is the area where the pocket implant junctions are in communication with a non-sidewall portion of the source and drain.

In combining the pocket implant junction of Wolf et al. with the raised source/drain structure of Moravvej-Farshi et al., the pocket implants would necessarily be formed in the substrate along the edges (and partially underneath) of the gate. In using the large-angle tilt implant in the self-aligned pocket implantation of Wolf et al. figure 5-25(c), the pocket implantation is aligned by the gate. In applying this method and the resulting implanted structure into Moravvej-Farshi et al., the pocket implants

would be formed in the substrate such that the pocket implants would be in communication with a non-sidewall portion of the source and drain.

Also, it is noted that a highly doped region in silicon (whether highly doped n-type or p-type) defines a low-resistance path as the addition of the n- or p- type dopants is known to lower the resistance of the material.

Moravvej-Farshi et al. and Wolf et al. are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to form a first and second pocket implant junction as claimed. The motivation for doing so is to suppress punchthrough effects in a short channel device allowing for a shorter channel length without subsurface punchthrough such that smaller channel lengths can be fabricated that still exhibited long-channel subthreshold behavior. Therefore, it would have been obvious to combine Moravvej-Farshi et al. with Wolf et al. to obtain the invention of claim 17.

With regard to claim 98, the raised source is doped polysilicon.

With regard to claim 99, the raised drain is doped polysilicon.

With regard to claim 100, the gate is doped polysilicon.

With regard to claim 101, the source includes a plug.

With regard to claim 103, the gate includes a gate terminal as the entire gate structure is considered the gate terminal.

With regard to claim 125, Moravvej-Farshi et al. disclose in figure 6 a raised drain structure (n+ poly), a raised source structure (n+ poly), a gate (n+ poly) located between the source and drain, a first capping layer (silicon dioxide on left half of figure) in

communication with at least a portion of the gate and source, a first portion of a gate oxide region in communication with at least a portion of the gate and source, a first outidffusion area (shown with dashed lines) located in the substrate assembly and extending under a second portion of the source, a second capping layer (silicon dioxide on right half of figure) in communication with at least a portion of the gate and drain, a second portion of a gate oxide region in communication with at least a portion of the gate and drain, and a second outdiffusion area (dashed line beneath drain) located in the substrate assembly extending under a second portion of the drain. Moravvej-Farshi et al. do not teach a first pocket implant junction located in the substrate assembly comprising a first high dose implant and defining a first low-resistance path wherein the first pocket implant junction is in communication with a non-sidewall portion of the source and extends under a first portion of the gate. Nor does Moravvej-Farshi et al. teach a second pocket implant junction located in the substrate assembly comprising a second high dose implant and defining a second low-resistance path wherein the second pocket implant junction is in communication with a non-sidewall portion of the drain and extends under a first portion of the gate.

Wolf et al. teach a transistor formed on a substrate assembly in figure 5-25(c), for example. Wolf et al. teach a source, drain, polysilicon gate between the source and drain, a gate oxide, and first and second pocket implant junctions. As seen in figure 5-25(c) P-type pocket implant junctions are formed in the substrate assembly by first and second high dose implants, thus defining a low-resistance path, and the pocket implant junctions are in communication with a non-sidewall portion of the source and drain and

extend under a portion of the gate. As seen in figure 5-25(c), the p+ pocket implants extend a short distance under the source and drain, this short distance is the area where the pocket implant junctions are in communication with a non-sidewall portion of the source and drain.

In combining the pocket implant junction of Wolf et al. with the raised source/drain structure of Moravvej-Farshi et al., the pocket implants would necessarily be formed in the substrate along the edges (and partially underneath) of the gate. In using the large-angle tilt implant in the self-aligned pocket implantation of Wolf et al. figure 5-25(c), the pocket implantation is aligned by the gate. In applying this method and the resulting implanted structure into Moravvej-Farshi et al., the pocket implants would be formed in the substrate such that the pocket implants would be in communication with a non-sidewall portion of the source and drain..

Also, it is noted that a highly doped region in silicon (whether highly doped n-type or p-type) defines a low-resistance path as the addition of the n- or p- type dopants is known to lower the resistance of the material.

Moravvej-Farshi et al. and Wolf et al. are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to form a first and second pocket implant junction as claimed. The motivation for doing so is to suppress punchthrough effects in a short channel device allowing for a shorter channel length without subsurface punchthrough such that smaller channel lengths can be fabricated that still exhibited long-channel

subthreshold behavior. Therefore, it would have been obvious to combine Moravvej-Farshi et al. with Wolf et al. to obtain the invention of claim 125.

With regard to claim 126, though Moravvej-Farshi et al. do not specifically teach forming the device of figure 6 as a P-channel device, it would have been obvious to one of ordinary skill in the art to form the device with opposite conductivity types than shown to form a PMOS. In doing so and applying the teaching of Wolf et al. to suppress punchthrough effects it would have been obvious to one of ordinary skill in the art to form the first and second pocket implant junctions with phosphorous. Wolf et al. teach doping with phosphorous in a PMOS device to form pocket implants on page 238, final paragraph.

With regard to claim 128, Moravvej-Farshi et al. disclose in figure 6 a raised drain structure (n+ poly), a raised source structure (n+ poly), a gate (n+ poly) located between the source and drain, a first capping layer (silicon dioxide on left half of figure) in communication with at least a portion of the gate and source, a first portion of a gate oxide region in communication with at least a portion of the gate and source, a second capping layer (silicon dioxide on right half of figure) in communication with at least a portion of the gate and drain, and a second portion of a gate oxide region in communication with at least a portion of the gate and drain. Moravvej-Farshi et al. do not teach a halo structure in the substrate assembly comprising a first pocket implant junction and a second pocket implant junction, first pocket implant junction comprising a first high dose implant in communication with a non-sidewall portion of the source and extends under a first edge of the gate and the second pocket implant junction

comprising a second high dose implant in communication with a non-sidewall portion of the drain and extends under a second edge of the gate.

Wolf et al. teach a transistor formed on a substrate assembly in figure 5-25(c), for example. Wolf et al. teach a source, drain, polysilicon gate between the source and drain, a gate oxide, and a halo implant structure including first and second pocket implant junctions. As seen in figure 5-25(c) P-type pocket implant junctions are formed in the substrate assembly by first and second high dose implants, thus defining a low-resistance path, and the pocket implant junctions are in communication with a non-sidewall portion of the source and drain and extend under a portion of the gate. As seen in figure 5-25(c), the p+ pocket implants extend a short distance under the source and drain, this short distance is the area where the pocket implant junctions are in communication with a non-sidewall portion of the source and drain.

In combining the pocket implant junction of Wolf et al. with the raised source/drain structure of Moravvej-Farshi et al., the pocket implants would necessarily be formed in the substrate along the edges (and partially underneath) of the gate. In using the large-angle tilt implant in the self-aligned pocket implantation of Wolf et al. figure 5-25(c), the pocket implantation is aligned by the gate. In applying this method and the resulting implanted structure into Moravvej-Farshi et al., the pocket implants would be formed in the substrate such that the pocket implants would be in communication with a non-sidewall portion of the source and drain.

Moravvej-Farshi et al. and Wolf et al. are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a

person of ordinary skill in the art to form a first and second pocket implant junction as claimed. The motivation for doing so is to suppress punchthrough effects in a short channel device allowing for a shorter channel length without subsurface punchthrough such that smaller channel lengths can be fabricated that still exhibited long-channel subthreshold behavior. Therefore, it would have been obvious to combine Moravvej-Farshi et al. with Wolf et al. to obtain the invention of claim 128.

3. Claim 102 is rejected under 35 U.S.C. 103(a) as being unpatentable over Moravvej-Farshi et al. ("Novel Self-Aligned Polysilicon-Gate MOSFETs with Polysilicon Source and Drain," Solid-State Electronics, Vol. 30, No. 10, 1987, Pp. 1053-62) with Wolf et al. ("Silicon Processing for the VLSI Era, Volume 3: The Submicron MOSFET," 1995, Pp. 232-240 and 309-311) as applied to claims 17, 98-101, 103, 125, 126 and 128 above in view of Iio et al. (U.S. Patent No. 6,130,482).

Moravvej-Farshi et al. teach a plug on the source but do not teach an adhesive layer included in the plug. The plug of Moravvej-Farshi et al. is taught as comprising aluminum and the source region is silicon. Iio et al. teach an aluminum plug in a contact hole where the aluminum plug contacts a silicon substrate (figure 3C, column 9 lines 38-46 and column 10 lines 35-50). Iio et al. teach forming a TiN adhesion/barrier layer between the aluminum plug and the silicon substrate.

Moravvej-Farshi et al. with Wolf et al. and Iio et al. are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to form an adhesion/barrier layer between

the plug and the silicon source. The motivation for doing so is to prevent junction spiking (see Iio et al. column 10 lines 44-50). Therefore, it would have been obvious to combine Moravvej-Farshi et al. and Wolf et al. with Iio et al. to obtain the invention of claim 102.

Response to Arguments

4. Applicant's arguments filed 12/22/04 have been fully considered but they are not persuasive.

Applicant has argued that the none of the references applied in the previous rejections taught the claimed pocket implant junctions that are in communication with a non-sidewall portion of the source/drain since Wolf et al. teaches the "halo implant" raising the doping concentration only on the inside walls of the source/drain junctions, i.e. only on the sidewall portions. This is not persuasive for two reasons. First, Wolf et al. teach in figure 5-25(c) a large-angle tilt implant to form a halo-like structure where, as shown in figure 5-25(c), the implant does extend a small distance under the source/drain region such that it is in communication with a non-sidewall portion of the source/drain. Second, in combining Wolf et al. with Moravvej-Farshi et al., the halo or halo-like implants into the substrate along the edge of the channel region as taught by Wolf et al. would be formed in the substrate of Moravvej-Farshi et al., and thus using the large angle tilt implant they would be in communication with a non-sidewall portion of the source/drain regions. Thus, in combining the references, the claimed pocket implant junctions are obvious.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to N. Drew Richards whose telephone number is (571) 272-1736. The examiner can normally be reached on Monday-Friday 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NDR

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER